REMARKS

Applicant herein amends the specification in order to correct reference numeral errors. No new matter has been added to the specification. Entry of the specification amendments is requested.

Claims 1-13, 15, 17, 19 and 21-32 are all the claims presently pending in the application.

Applicant herein amends claims 30-32. The amended claims 30-32 are now similar in scope to claims 27-29, and the amendments to claims 30-32 add no new matter. In addition, the amendments to claims 30-32 do not raise any new issues requiring a further search by the Examiner, and reduce the issues for appeal. Entry of the amendments to claims 30-32 is requested.

1. As a preliminary matter, there are several outstanding errors and omissions that Applicant wishes to address:

a. The Office Action Summary is incorrect as claim 18 was cancelled without prejudice and/or disclaimer in the November 15, 2001 Amendment.

b. The Examiner indicates that claims 2, 4-7, 9, 11, 15, 17-19, 24 and 30-32 are withdrawn from consideration. As noted above, claim 18 was cancelled in the November 15, 2001 Amendment.

2. Claims 30-32 are withdrawn from consideration pursuant to 37 C.F.R. § 1.142(b) as allegedly being drawn to non-elected embodiments.

Applicant traverses the Examiner's withdrawal as being unnecessary and unsupportable. The subject matter of claims 30-32 is readable on the elected species, and, in fact, is discussed in the text

that describes the elected species. *See* page 18, lines 3-6 of the specification. The Examiner has made no showing that claims 30-32 do not read on the elected species. Moreover, claims 30-32 do not recite a particular structure for the bipolar transistor, the thyristor or the diode. Should someone not be familiar with bipolar transistors, thyristors and diodes, the other embodiments are relevant, if only to verify that at least the inventor was using the phrases "bipolar transistor," "thyristor." and "diode" consistently with their plain and ordinary meaning. However, such disclosure is not required in order for claims 30-32 to be readable on the elected species, in view of the rudimentary nature of the elements claimed, and the clear recitation of the elements in the discussion of the elected embodiment. Applicant requests that claims 30-32 be reinstated under 37 C.F.R. § 1.142(b).

3. Claims 9 and 24 remain withdrawn from consideration as being drawn to a non-elected embodiment.

Applicant traverses the Examiner's withdrawal as being unnecessary as well as unsupportable. The subject matter of claims 9 and 24 is readable on the elected species, and, in fact, is discussed in the text that describes the elected species. *See* page 18, lines 20-23 of the specification. The text even discusses the connection of the power source wire (10) to a predetermined source voltage or connected to a source voltage conversion circuit. It is well settled that patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661 (Fed. Cir. 1991). Connecting a power source to a power source wire is well within the grasp of one of ordinary skill in the art. Should someone not be familiar with predetermined source voltages or source voltage conversion circuits, the embodiment shown in Figure 2 is relevant,

if only to verify how the inventor was using the phrases "predetermined source voltage" or "source voltage conversion circuit." However, such disclosure is not required in order for claims 30-32 to be readable on the elected species, in view of the rudimentary nature of the elements claimed, and the clear recitation of the elements in the discussion of the elected embodiment. The Examiner has made no substantive showing that claims 9 and 24 do not read on the elected species. The Examiner's Response to Applicant's arguments is not well taken in that Figure 2 simply shows the connection between the internal circuit (20) and a power source. *See* August 23, 2002 Office Action, pg. 7, numbered paragraph 8. The Examiner's argument that Figure 2 somehow depicts a different invention than the elected species is without merit, and the Examiner's argument that Applicant did not elect to prosecute Figure 2 now somehow prevents its use in depicting well-known art is even more puzzling.[1] Applicant requests that claims 9 and 24 be reinstated under 37 C.F.R. § 1.142(b). **If the Examiner does not intend to reinstate claims 9 and 24, the Examiner is kindly requested to set forth an explanation that includes relevant Federal Circuit citations and/or MPEP sections supporting the Examiner's position.**

4. Claims 27-29 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly containing subject matter that was not described in the specification. Applicant traverses the rejection of claims 27-29 at least for the reasons set forth below.

[1] In the February 21, 2001 Election of Species Requirement, Figure 2 is not even listed as one of the species to be elected. Figure 2 simply illustrates the connection of a power source to the internal circuit (20).

A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. *See, e.g., In re Marzocchi*, 439 F.2d 220, 224 (CCPA 1971). The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. *In re Wertheim*, 541 F.2d 257, 263 (CCPA 1976).

The Examiner's repeated rejection of claims 27-29 under 35 U.S.C. § 112, first paragraph is clearly unreasonable in light of *Marzocchi* and *Wertheim*, and is contrary to the guidelines set forth at MPEP § 2163.04. The Examiner has failed to provide any probative evidence that the description would not convey to one skilled in the art that the inventor was in possession of the invention at the time the application was filed. Thus, Applicant believes that the Examiner has failed to make a *prima facie* case as required under MPEP § 2163.04 (I)(B) and *In re Wertheim*.

Contrary to the Examiner's statement at page 3, numbered paragraph 4 of the August 23, 2002 Office Action, the specification states that, for the first embodiment, the electrostatic protection element can be a bipolar transistor, a thyristor or a non-parasitic diode. *See* page 18, lines 3-6 of the instant specification. In the August 23, 2002 Office Action, there is no explanation as to why one of ordinary skill in the art would not understand that the inventor was in possession of the invention at the time of the filing of the application. It is well settled that patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661 (Fed. Cir. 1991). Instead, in the Response to Applicant's arguments, the Examiner responds that Applicant admits the use of

a bipolar transistor, a thyristor or a diode in Figures 4-14 of the instant application. With respect to Figure 1, the specification states as follows:

> This electrostatic protection element 18 is, for example, a MOS field effect transistor, the drain of which is connected to the power source wire 10 and the source and gate of which are connected to the ground potential wire 12. It is noted that the electrostatic protection element is not limited to a field effect transistor, but a bipolar transistor, a thyrister or a diode (excluding a parasitic diode) may be used as the electrostatic protection element 18.

Page 17, line 23 to page 18, line 6 of the instant specification.

Thus, based on the above disclosure, Applicant can discern no reasonable basis for the Examiner's argument that the use of a bipolar transistor, a thyristor or a diode as an electrostatic protection element would not be understood by one of ordinary skill in the art.

In fact, if one of ordinary skill in the art reads the specification, it would be readily apparent that the inventor was in possession of the invention at the time of the filing of the application. To illustrate, the first embodiment of the invention (see Figure 1 of the instant application) and the third embodiment of the invention (see Figure 4 of the instant application) share an identical circuit structure *vis-à-vis* the electrostatic protection element (18) and the MOS capacitor (16). Figures 9 and 10 and the accompanying text describe the construction of a bipolar transistor (electrostatic protection element 18) and a MOS capacitor (16) for the third embodiment of the invention. *See* Figures 9 and 10; page 27, line 14 to page 28, line 14 of the instant specification. Figures 11 and 12 and the accompanying text describe the construction of a non-parasitic diode (electrostatic protection element 18) and a MOS capacitor (16) for the third embodiment of the invention. *See* Figures 11 and 12; page 28, line 15 to page 29, line 3 of the instant specification. Figures 13 and

14 and the accompanying text describe the construction of a thyristor (electrostatic protection element 18) and a MOS capacitor (16) for the third embodiment of the invention. *See* Figures 13 and 14; page 29, line 3 to page 30, line 2 of the instant specification. The reference numbers for the electrostatic protection element and MOS capacitor shown in Figure 1 are no different than the reference numbers for the electrostatic protection element and MOS capacitor shown in Figures 4 and 9-14. *See* 37 C.F.R. § 1.84(p)(4) (same reference numbers are used for identical parts in different views). In sum, with respect to the elected embodiment, the written description and the drawings disclose an electrostatic protection element that can be a bipolar transistor, a thyristor or a non-parasitic diode.

Previously, the Examiner argued that the written description for a non-elected claim could not be used to provide support for an element of an elected claim. *See* Final Office Action dated August 15, 2001, page 5, numbered paragraph 6. However, it is clear that the electrostatic protection element (18) and the MOS capacitor (16) illustrated in Figure 1 are identical to the electrostatic protection element (18) and the MOS capacitor (16) depicted in Figure 4. These Figures are original, and have not been amended in any way. Again, Applicant notes that the Examiner has not identified any relevant Federal Circuit caselaw citation, Title 37 C.F.R. section or MPEP section that supports his position.

"An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention." MPEP § 2163(I). "Generally, there is an inverse correlation between the level of skill and knowledge in the art and the specificity of the

written description requirement." MPEP § 2163(II)(A)(2). Even if relying solely on the description explicitly describing the first embodiment, the mere identification of element (18) as being a bipolar transistor, thyristor or a diode is sufficient to support claims 27-29. The recited components are ubiquitous in the art, and have been for decades. Applicant believes that this description of the circuit, in combination with illustration and discussion of Figure 1 are all that is required to put the public in possession of the invention and to enable those skilled in the art to make and use the invention.

Moreover, claims 27-29 do not recite a particular structure bipolar transistor, thyristor or a diode. Should someone not be familiar with bipolar transistors, thyristors and diodes, the other embodiments are relevant, if only to verify that at least the inventor was using the phrases "bipolar transistor," "thyristor," and "diode" according to their plain and ordinary meaning. However, such disclosure is not required in order for claims 27-29 to be patentable, in view of the rudimentary nature of the elements claimed, and the clear recitation of the elements in the discussion of the elected embodiment.

Thus, Applicant believes that the Examiner is being unreasonable that one skilled in the art of semiconductor manufacturing would not understand that a bipolar transistor, a thyristor or a non-parasitic diode could be used as the electrostatic protection element. Applicant requests that the Examiner withdraw the § 112, first paragraph rejection.

5. Claims 3, 8, 10, 12 and 13 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. Applicant notes that claim 13 depends from claims 4 and 5, neither of which were elected for prosecution.

As argued previously, the rejection of claims 3, 8, 10 and 12 is premature. Claims 3, 8, 10 and 12 are multiple dependent claims that depend from claims 1 and 2. Claim 1 was elected for prosecution on the merits and has been indicated as generic by the Applicant in the Response to Election of Species Requirement filed on March 21, 2001. The claims are not rendered indefinite because they depend from both elected and non-elected species. Therefore, it is unnecessary to consider the metes and bounds of claims 3, 8, 10 and 12 with respect to claim 2. Claim 2 has been withdrawn from consideration, and the form of claims 3, 8, 10 and 12 depending from non-elected claim 2 should simply be considered as withdrawn claims. The Examiner appears to be confusing an Election of Species Requirement with a Restriction Requirement. At present, no burden has been placed on Applicant to file a divisional application with respect to the non-elected claims. Again, Applicant requests that the Examiner withdraw the § 112 rejection as premature.

6. Claims 1, 3, 8, 10, 12, 13, 21-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. (U.S. Patent No. 4,456,939) in view of Miller (U.S. Patent No. 5,255,146). Applicant notes that claim 13 depends from claims 4 and 5, neither of which were elected for prosecution. Applicant traverses the rejection of claims 1, 3, 8, 10, 12, 21-23 and 25-29 for at least the reasons set forth below.

The Examiner again acknowledges that Ozaki et al. fails to teach or suggest that the wire resistance of the ground potential wire between the ESD element connection point and the ground terminal is larger that the wire resistance of the ground potential wire between the ESD element connection point and the MOS capacitor connection point. *See* numbered paragraph 7, page 4 of the Office Action dated August 23, 2002. In the Response to Arguments section, the Examiner states that, in previous Office Actions, Cohn et al. (U.S. Patent No. 5,535,134) supports the position that it is well known to use computers in the design of integrated circuit layouts. *See* numbered paragraph 8, page 6 of the Office Action dated August 15, 2001. However, in the Amendment filed on January 15, 2002, Applicant noted that in the passage cited by the Examiner, all that Cohn et al. state is that computers can be used for the layout of objects in a semiconductor layout, and Applicants further noted that Cohn et al. is silent with respect to the claimed resistance relationship recited in claim 1. *See* Amendment Under 37 C.F.R. § 1.111 filed on January 15, 2002, pages 5-7.

The Examiner combines Ozaki et al. with Miller in an attempt to overcome the acknowledged deficiencies of Ozaki et al. Figure 2 of Miller depicts a plurality of ESD protection circuits 14 connected between a V_{DD} ring and a V_{SS} ring.

The initial burden of establishing that a claimed invention is *prima facie* obvious rests on the USPTO. *In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984). To make its *prima facie* case of obviousness, the USPTO must satisfy three requirements:

1. The prior art relied upon, coupled with the knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated to artisan to modify a reference or to combine references. *In re Fine*, 837 F.2d 1071, 1074

(Fed. Cir. 1988).

2. The proposed modification of the prior art must have had a reasonable expectation of success, and that determined from the vantage point of the artisan at the time the invention was made. *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1209 (Fed. Cir. 1991).
3. The prior art reference or combination of references must teach or suggest all the limitations of the claims. *In re Vaeck*, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991); *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, the nature of a problem to be solved. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). Alternatively, the motivation may be implicit from the prior art as a whole, rather than expressly stated. *Id.* Regardless if the USPTO relies on an express or an implicit showing of motivation, the USPTO is obligated to provide particular findings related to its conclusion, and those findings must be clear and particular. *Id.* A broad conclusionary statement, standing alone without support, is not "evidence." *Id.; see also, In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001).

In addition, a rejection cannot be predicated on the mere identification of individual components of claimed limitations. *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000). Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *Id.*

The combination of Ozaki et al. and Miller fails to teach or suggest that the wire resistance of a ground wire portion between an electrostatic protection element and a ground terminal is larger than a wire resistance of the ground wire portion between the electrostatic protection element and a MOS capacitor, as recited in independent claims 1 and 21. In Figure 2 of Miller and its accompanying text, there is no indication that the ESD protection circuit 14 is positioned relative to a MOS capacitor such that the resistive relationship as recited in claim 1 is taught or suggested. The Examiner simply states that Figure 2 of Miller shows the claimed resistive relationship, without any further support as to how one of skill in the art would derive that teaching from Miller. The Examiner has not pointed to any teaching or suggestion in Miller, when combined with Ozaki et al., that would teach or suggest the claimed resistance relationship between an electrostatic protection device and a capacitor recited in independent claims 1 and 21. Therefore, combination of references fails to show the claimed resistance relationship between an electrostatic protection device and a capacitor, as recited in independent claims 1 and 21.

Moreover, the figures of Miller do not support an obviousness rejection. "When the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value." MPEP § 2125. "[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." MPEP § 2125 *quoting Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000). Thus, since the Examiner is not entitled to rely upon the figures in Miller to provide any teaching

with respect to the resistive relationship between the recited elements, the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness has not been satisfied.

Again, the Examiner has not made any findings on the record, as required by *Dembiczak*, as to why one of ordinary skill in the art would be motivated to combine Ozaki et al. and Miller. Thus, the motivation prong of a *prima facie* case of obviousness has not been satisfied. Therefore, Applicant maintains that the Examiner has not set forth a *prima facie* case of obviousness with respect to independent claims 1 and 21, as required by *Piasecki*.

Finally, with respect to the Examiner's argument that computers are routinely used to design integrated circuit layouts the Examiner is obligated to provide concrete evidence in the record to support his assertion that it is well within the skills of an artisan to find the optimum layout of the Applicant's device by using computers. *See In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001). The Examiner cannot simply reach conclusions based upon his own assessment of what would be basic knowledge or common sense. *Id.* With respect to design choice, only the simple repositioning of isolated components has ever been found to be covered by the umbrella of "design choice" and not the specific arrangement of cooperative elements. *In re Japikse*, 86 U.S.P.Q. 70 (C.C.P.A. 1950)(the repositioning of an actuating switch from one physical location to another cannot be the basis of patentability for a hydraulic press).

Thus, Applicant believes that independent claims 1 and 21 are allowable over the combination of Ozaki et al. and Miller, and Applicant further believes that claims 3, 8, 10, 12, 21-23 and 25-29 at least by virtue of their dependency from claims 1 and 21, respectively.

7. Claims 1, 3, 8, 10, 12, 13, 21-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. in view of Puar (U.S. Patent No. 4,786,956). Applicant notes that claim 13 depends from claims 4 and 5, neither of which were elected for prosecution. Applicant traverses the rejection of claims 1, 3, 8, 10, 12, 21-23 and 25-29 for at least the reasons set forth below.

The Examiner combines Puar with Ozaki et al. in an attempt to overcome the deficiencies of Ozaki et al. with respect to the resistance relationship recited in independent claims 1 and 21. The Examiner alleges that Puar depicts an ESD circuit (16) being located closer to an integrated circuit (10) than to a ground terminal such that the ground wire resistance between the ESD circuit (16) and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit (16) and the ground connection point.

Again, Applicant submits that the Examiner has failed to make a *prima facie* case of obviousness as required by *Piasecki*. The Examiner has not made any findings on the record, as required by *Dembiczak*, as to why one of ordinary skill in the art would be motivated to combine Ozaki et al. and Puar. The record simply lacks any discussion of motivation whatsoever. Thus, the motivation prong of a *prima facie* case of obviousness has not been satisfied.

In addition, the Examiner has not cited any teaching or suggestion in Puar, when combined with Ozaki et al., that would teach or suggest the claimed resistance relationship between an electrostatic protection device and a capacitor recited in independent claims 1 and 21. The Examiner simply states that Figure 1 of Puar shows the claimed resistive relationship, without any further support as to how one of skill in the art would derive that teaching from Puar. Puar is replete with diagrams

of the ESD circuit (16), but there is no teaching or suggestion of the resistance relationship between an ESD element, a capacitor and a ground terminal as recited in independent claims 1 and 21. Moreover, the Examiner's statement that Figure 1 of Puar shows the claimed resistive relationship does not make sense, since no ground wire paths are even depicted. Similar to Miller, the figures of Puar do not support an obviousness rejection. *See* MPEP § 2125 *quoting Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000). Thus, since the Examiner is not entitled to rely upon the figures in Puar to provide any teaching with respect to the resistive relationship between the recited elements, the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness has not been satisfied. Therefore, Applicant maintains that the Examiner has not set forth a *prima facie* case of obviousness with respect to independent claims 1 and 21, as required by *Piasecki*.

Thus, Applicant believes that independent claims 1 and 21 are allowable over the combination of Ozaki et al. and Puar, and Applicant further believes that claims 3, 8, 10, 12, 21-23 and 25-29 at least by virtue of their dependency from claims 1 and 21, respectively.

8. Claims 1, 3, 8, 10, 12, 21-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. in view of Igarashi (U.S. Patent No. 4,656,491). Applicant notes that claim 13 depends from claims 4 and 5, neither of which were elected for prosecution. Applicant traverses the rejection of claims 1, 3, 8, 10, 12, 21-23 and 25-29 for at least the reasons set forth below.

The Examiner combines Igarashi with Ozaki et al. in an attempt to overcome the deficiencies of Ozaki et al. with respect to the resistance relationship recited in independent claims 1 and 21. The Examiner alleges that Igarashi depicts an ESD circuit being located closer to an integrated circuit than to a ground terminal such that the ground wire resistance between the ESD circuit and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit and the ground connection point.

Applicant submits that the Examiner has failed to make a *prima facie* case of obviousness as required by *Piasecki*. The Examiner has not made any findings on the record, as required by *Dembiczak*, as to why one of ordinary skill in the art would be motivated to combine Ozaki et al. and Igarashi. Again, the record simply lacks any discussion of motivation whatsoever. Thus, the motivation prong of a *prima facie* case of obviousness has not been satisfied.

In addition, the Examiner has not cited any teaching or suggestion in Igarashi, when combined with Ozaki et al., that would teach or suggest the claimed resistance relationship between an electrostatic protection device and a capacitor recited in independent claims 1 and 21. In fact, the Figures cited by the Examiner show the opposite of the claimed resistive relationship. To illustrate, the resistor (R12) is connected between the transistors Q11-Q1n. *See* Fig. 4 of Igarashi. However, there is very little resistance between the ground terminal (103) and the transistor Q1n. This resistive relationship is opposite to the resistive relationship recited in independent claims 1 and 21. *See W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540 (Fed. Cir. 1983) (prior art reference must be considered in its entirety, including portions that would teach away from the claimed invention). Similar to Miller, the figures of Igarashi do not support an obviousness

rejection, and the Examiner's statement in the Response to Arguments section indicates that the Examiner is relying upon the figures as support for the obviousness rejection. *See* MPEP § 2125 *quoting Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000). Thus, since the Examiner is not entitled to rely upon the figures in Igarashi to provide any teaching with respect to the resistive relationship between the recited elements, the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness has not been satisfied. Applicant believes that the Examiner has failed to satisfy the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness as well, since it is apparent that the combination of Igarashi with Ozaki et al. discloses a resistive relationship that is opposite to the claimed resistive relationship. Therefore, Applicant maintains that the Examiner has not set forth a *prima facie* case of obviousness with respect to independent claim 1, as required by *Piasecki*.

Thus, Applicant believes that independent claims 1 and 21 are allowable over the combination of Ozaki et al. and Igarashi, and Applicant further believes that claims 3, 8, 10, 12, 21-23 and 25-29 at least by virtue of their dependency from claims 1 and 21, respectively.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 6, second full paragraph:

Similarly, in the semiconductor integrated circuit device 201', the discharge speed of the charge charged in the ground potential wire 202 from the input/output terminal 212 [202] through the electrostatic protection element 214 is slower than the discharge speed of the charge charged in the power source wire 200 from the input/output terminal 212 through the circuit elements, a potential difference ΔV is generated between both terminals of the MOS capacitor 206. If the potential difference ΔV exceeds the electrostatic breakdown voltage, the MOS capacitor 206 is subjected to the electrostatic breakdown.

Paragraph bridging pages 17 and 18:

An electrostatic protection element (CDM protection element) 18 is provided between the ground terminal 14 and the MOS capacitor 16 in parallel to the MOS capacitor 16 [18]. This electrostatic protection element 18 has a function of clamping the voltage generated between both terminals of the MOS capacitor 16 at the time of the CDM test be a voltage lower than the dielectric breakdown voltage. This electrostatic protection element 18 is, for example, a MOS field effect transistor, the drain of which is connected to the power source wire 10 and the source and gate of which are connected to the ground potential wire 12. It is noted that the electrostatic protection

element is not limited to a field effect transistor, but a bipolar transistor, a thyrister or a diode (excluding a parasitic diode) may be used as the electrostatic protection element 18.

Page 28, second full paragraph:

Furthermore, as shown in Fig. 9, a bipolar transistor is constituted by closely forming N^+ diffusion layers 74 and 76 so as to face each other. This bipolar transistor constitutes electrostatic protection element 32, the N^+ diffusion layer 74 connected to the ground potential wire 12, and the N^+ diffusion layer 76 is connected to the input/output terminal 30. As shown in Fig. 9, a wire 34 to the internal circuit 20 [34] is connected to the input/output terminal 30 in addition to the electrostatic protection element 32.

IN THE CLAIMS:

The claims are amended as follows:

30. (*Amended*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a bipolar transistor [that comprises a substrate having a first conductive type and two diffusion layers having a second conductive type which is an opposite conductive type to the first conductive type, said two diffusion layers disposed so as to closely face each other].

31. (*Amended*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a thyristor [that comprises a substrate having a first conductive type and two diffusion layers respectively having a first conductive type and a second conductive type, an opposite conductive type to the first conductive type, so as to closely face each

other, and by further forming on a well having the second conductive type provided on said substrate having the first conductive type two diffusion layers respectively having the first conductive type and the second conductive type, so as to closely face each other].

32. (*Amended*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a diode [that comprises a substrate or a well having a first conductive type and two diffusion layers having a second conductive type which is an opposite conductive type to the first conductive type, said two diffusion layers disposed so as to closely face each other].